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14. ABSTRACT
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Tbit/s optical packet processing using the resonant soliton logic gates

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Abstract

Optical packet processing is emerging as one of the key technologies for implementation of future ultra-high-speed and multi-functional TDM networks. An essential element of these networks is a receiver node with functionalities which include packet address recognition, packet routing, buffering and rate conversion. In this research program, a possibility of Tbit/s optical packet processing in a TDM receiver node using the resonant soliton switches and logic gates has been demonstrated. The address recognition function for incoming optical packets has been performed numerically at 2 Tbit/s and 200 Gbit/s data rates. Buffering of optical packets to produce multiple copies of the inputs has been modelled using 3×3 nonlinear directional coupler configuration; the simulations have been performed at two different data rates: 3 Tbit/s and 500 Gbit/s. A simple scheme to upconvert the repetition rate of an optical clock stream has been proposed, and the repetition rate multiplication from 250 Gbit/s to 1 Tbit/s has been demonstrated. A possible scheme to achieve the data rate down-conversion in the case of optical packets of arbitrary format has been described. The examples of demultiplexing of optical clock streams and optical packets at 3 Tbit/s have been presented. The operating characteristics of the components in the receiver node have been assessed. To our knowledge, this is the first demonstration of the possibility of optical packet processing at Tbit/s data rates.

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Content

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1. Outline of the completed tasks

Photonic packet processing is emerging as one of the key technologies for implementation of future high-capacity and multi-functional optical communication networks. The aim of this project is to demonstrate numerically that ultra-high-speed photonic packet processing in time-division-multiplexed (TDM) networks can be realized using the resonant soliton switches and logic gates. The main advantage of the resonant soliton scheme for optical switching is that it allows to achieve throughput in the terabit per second range with high performance [1,2].

An essential element of ultra-high-speed optical TDM networks is a receiver node with functionalities which include packet address recognition, packet routing, buffering and rate conversion. In the performed research program, a feasibility to construct a receiver node using the resonant soliton switches and logic gates has been demonstrated. The address recognition function for incoming optical packets has been performed numerically at 2 Tbit/s and 200 Gbit/s data rates. The header processor operation has been modelled in the cases when the incoming address matches and does not match the local address. Buffering of optical packets to produce multiple copies of the inputs has been performed using 3×3 nonlinear directional coupler (NLDC) configuration; the simulations have been performed at two different data rates: 3 Tbit/s and 500 Gbit/s. A simple scheme to upconvert the repetition rate of an optical clock stream has been proposed, and the repetition rate multiplication from 250 Gbit/s to 1 Tbit/s has been demonstrated. A possible scheme to achieve the data rate down-conversion in the case of optical packets of arbitrary format has been described. The examples of demultiplexing of optical clock streams and optical packets at 3 Tbit/s have been presented. The operating characteristics of the components in the receiver node have been assessed. To our knowledge, this is the first demonstration of the possibility of optical packet processing at Tbit/s data rates.

2. Overview of various approaches to optical networking and packet switching

Ultra-high-speed optical TDM systems may offer unique advantages over wavelength-division-miltiplexed (WDM) networks. The latter ones divide the fiber bandwidth into a large number of channels, distinguished by wavelength, each operating at electronic rates (typically up

to about 10 Gbit/s per channel). A review of photonic packet switching with emphasis on WDM techniques can be found in Ref. [3].

One of the approaches to TDM networking is so-called bit-interleaved TDM where data from several sources, each at the rate less than the full channel rate, are multiplexed up to the channel rate. From the perspective of the network, this is similar to WDM approach as each low-rate TDM channel is comparable to each WDM wavelength.

An alternative method which is of interest here, is fundamentally different from WDM and bit-interleaved TDM and is referred to as slotted TDM [4]. There, time is divided into slots of many bits (10–100 Kbit per slot). Users insert packets into these slots whenever empty slots are available. The data rate within the packets can be as high as the channel rate, potentially, in Tbit/s range. The use of this packet-based approach with a single ultrafast channel offers a number of advantages, such as: (i) simpler management and control (single stream vs. many wavelength channels); (ii) truly flexible band-width-on-demand; (iii) an ability to provide integrated services (including packet service); (iv) scalability in number of users (packet address space); (v) the use of digital processing. However, the deployment of TDM systems has been limited so far, mostly because the technologies needed to implement these networks are still in research stage, and also because of the existing challenges in scaling these systems to the wide area [4].

The ultrafast TDM network architecture suitable for local and metropolitan areas networks (LANs and MANs) has been described in Ref. [5]. This is so-called helical local area network (HLAN) which was originally intended for slotted TDM LANs and MANs with channel rates of 100+ Gbit/s. In HLAN, each packet consists of a header and a payload. The header contains addressing information and may contain additional control information. The whole packet duration is less than a slot time. The use of fixed length packets may significantly simplify the implementation of packet content resolution and buffering, packet routing, as well as packet synchronization.

Fig. 1 shows a schematic diagram of some of the hardware components needed to implement HLAN. This diagram also shows the functionalities of the receiver node, but the components in the transmitter node are nearly identical. These components are located at the interface between the optical bus and the local node electronics and must operate at the optical bus rate. The components

include ultrafast optical switches and logic gates, optical buffers, and rate converters; the logic gates are likely to utilize 100+ GHz optical clock sources for switching and synchronization.

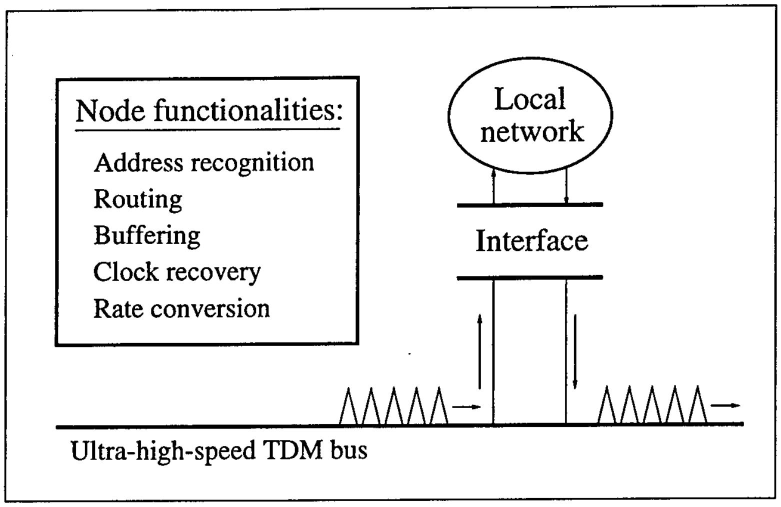

FIG. 1. Block diagram of an optical TDM bus used for long-distance interconnection of large regional networks, a local network, and an interface between them. Located at the interface is a receiver node which has a number of functionalities.

The presently available technologies for optical packet processing at the data rates exceeding 100 Gbit/s are extremely limited. A few gates and single buffers have been demonstrated at the research level, but there is no convenient low-loss variable optical delay, and there is no optical equivalent of a digital regenerator. To our knowledge, there has been only one laboratory demonstration of optical demultiplexing at bit rates in excess of 1 Tbit/s using symmetric Mach-Zehnder (SMZ) all-optical switch [6] (see Appendix). In our numerical work, a different approach to achieve Tbit/s all-optical switching has been recently proposed: the resonant soliton scheme [1]. Using this scheme, the operation of a variety of optical logic gates in Tbit/s regime has been modelled [2]. An experimental effort is currently underway to fabricate and test the resonant soliton NLDCs [7] (see Appendix). In the present research program, we demonstrate numerically that the resonant soliton switches and logic gates can be used for Tbit/s optical packet processing in TDM networks. In the next Section, a numerical method which has been adopted in the simulations is discussed.

3. Numerical method

A basic numerical code describing the operation of a semiconductor NLDC in the resonant excitation regime has been developed in our recent work where the inherent features of ultrafast all-optical resonant switching have been investigated [1]. This code applies to a directional coupler with two-arm branches (2×2 NLDC). The mathematical formalism is briefly described below.

Based on a coupled-mode approach, we solve the reduced Maxwell-semiconductor Bloch equations (MSBE) for single-mode waveguides in the case of resonant excitation at the $1s$-exciton resonance:

$$\frac{\partial E_j(\xi,\eta)}{\partial \xi} = i\frac{2\pi}{c^2}\frac{\omega_L^2}{k_L}P_j(\xi,\eta) + iKE_l(\xi,\eta), \tag{1}$$

$$\frac{\partial P_j(\xi,\eta)}{\partial \eta} = -i\left[\beta_1|P_j(\xi,\eta)|^2 - i\gamma_2\right]P_j(\xi,\eta) + \frac{id_{cv}}{2\hbar}\left[1-\beta_2|P_j(\xi,\eta)|^2\right]E_j(\xi,\eta), \tag{2}$$

where $E(\xi,\eta)$ and $P(\xi,\eta)$ are complex amplitudes of the electric field and the induced polarization in the moving coordinate frame ($\xi = z$ is the propagation coordinate, $\eta = t - z/U$ is the time coordinate, U is the group velocity of the pulse), β_1 and β_2 are nonlinear exchange and phase-space filling parameters, γ_2 is a phenomenological dephasing rate, $j,l = 1,2$ ($j \neq l$), and K is a coupling coefficient. The model assumes a large exciton binding energy, thus allowing higher exciton and continuum states to be neglected [8]. For femtosecond light pulses with moderate intensities, the neglect of screening is justified.

In the numerical simulations, the material parameters of II-VI CdZnTe/ZnTe MQWs [9] or III-V GaAs/AlGaAs MQWs [10] can be used. Here, similar to our previous work, II-VI CdZnTe/ZnTe MQWs parameters have been chosen [1,2]. It should be emphasized that the qualitative results do not depend on the choice of semiconductor material parameters. If III-V GaAs/AlGaAs MQWs material parameters are used, the carrier wavelength will be different, but only a minor quantitative change in the operating characteristics of the couplers (such as switching speed, switching contrast ratio, etc.) occurs.

Eqs. (1)–(2) can be solved using the fourth-order Runge-Kutta method which has been described in our previous work [1,8]. The input is given by various sequences of sech-shaped pulses

$E(\xi = 0, \eta) = E_0 sech(\eta/\tau)$; each pulse has 100 fs duration (intensity FWHM) and 2π pulse area. The interaction of the signal pulses in channel 1 and the control pulses in channel 2 of NLDC is monitored by computing the pulse intensity profile vs. time, the pulse energy, and the pulse area transmitted through each channel. If two or more NLDCs are cascaded, the same MSBE approach (1)–(2) can be used, where the output of the first NLDC serves as an input to the second NLDC, and so on.

In order to analyze the operation of a more complex three-arm branch (3×3) NLDC with three input ports and three output ports, an extended numerical code has been developed and tested in our recent work [2]. Although 3×3 device configuration is less conventional than 2×2 one, its functionality is higher. The coupled-mode equations describing 3×3 system are an extension of Eqs. (1)–(2), namely,

$$\frac{\partial E_1(\xi,\eta)}{\partial \xi} = i\frac{2\pi}{c^2}\frac{\omega_L^2}{k_L}P_1(\xi,\eta) + iKE_2(\xi,\eta) + iK'E_3(\xi,\eta), \tag{3}$$

$$\frac{\partial E_2(\xi,\eta)}{\partial \xi} = i\frac{2\pi}{c^2}\frac{\omega_L^2}{k_L}P_2(\xi,\eta) + iKE_1(\xi,\eta) + iKE_3(\xi,\eta), \tag{4}$$

$$\frac{\partial E_3(\xi,\eta)}{\partial \xi} = i\frac{2\pi}{c^2}\frac{\omega_L^2}{k_L}P_3(\xi,\eta) + iKE_2(\xi,\eta) + iK'E_1(\xi,\eta), \tag{5}$$

$$\frac{\partial P_j(\xi,\eta)}{\partial \eta} = -i\left[\beta_1|P_j(\xi,\eta)|^2 - i\gamma_2\right]P_j(\xi,\eta) + \frac{id_{cv}}{2\hbar}\left[1-\beta_2|P_j(\xi,\eta)|^2\right]E_j(\xi,\eta), \tag{6}$$

where $j = 1, 2, 3$; K' is a coupling coefficient between two outer waveguides (1 and 3), and the rest of the parameters are the same as in Eqs. (1)–(2). Eqs. (3)–(6) can be solved using the same procedure as in the case of Eqs. (1)–(2) (the fourth-order Runge-Kutta method).

In the performed numerical simulations, the operation of all-optical receiver node has been modelled. Its key components have been constructed using the resonant soliton switches and logic gates as building blocks. The operation of each switch/gate has been described either by Eqs. (1)–(2) or Eqs. (3)–(6) depending on whether 2×2 or 3×3 device configuration has been chosen. The numerical simulations have been performed using the existing computer facilities of the De-

partment of Theoretical Physics, Australian National University: Unix DEC Alpha Workstations with the operating speed up to 500 MHz.

4. Ultrafast optical packet processing in a receiver node using the resonant soliton switches and logic gates

The key components in a receiver node permit a number of functions, such as packet address recognition, packet routing, buffering and rate conversion. These components represent the network building blocks which operate at interface between the ultra-high-speed TDM packet networks and the local users (see Fig. 1).

Address recognition

The first function which must be performed in the receiver node is the packet address recognition (the header processing). Namely, the incoming packet address must be compared with the local address to determine whether or not the packet requires further processing. Address recognition must be performed at the optical bus rate of the ultra-high-speed TDM network. If the packet address matches the local address, the data packet must be stored while its rate converted down to the local user rate. If the incoming and local addresses do not match, the packet returns to the network.

Optical logic gates are crucial for address recognition function in the receiver node. Most of existing optical header processors suffer from slow processing speed for routing at required packet rates. Recently, the address recognition at 100 Gbit/s has been demonstrated with nonlinear optical loop mirrow (NOLM) logic gates [11]. For future TDM networks, the header processors operating in terabit per second range will be required. In our recent work, we have numerically investigated the operation of a new class of ultrafast optical logic devices – the resonant soliton logic gates featuring Tbit/s operating speed [2]. Namely, AND, OR, XOR, NOT, NOR and NAND logic gates have been modelled using 2×2 and 3×3 arm branching designs for a semiconductor NLDC. Using these results, it is now possible to model a receiver node which is capable of processing the optical packets at Tbit/s bit rates.

The schematic and operation of the receiver node which has been designed to perform the

functions of packet address recognition and packet routing at Tbit/s data rates, are shown in Figs. 2 and 3. The node consists of a buffer, an optical delay line, XOR gate, and a router. In the simulations, a 14-bit, 2-Tbit/s input optical packet with a 4-bit header and a 10-bit payload has been used (note that the choice of the packet length is arbitrary). The packet information has been coded with "1" bits (100-fs solitonlike pulses with the pulse area of 2π) and "0" bits (empty time intervals).

First, the input packet enters the buffer which creates two half-amplitude copies of the packet (see Fig. 2). One copy is directed to XOR gate for header processing, another copy passes through the optical delay line during the time required to complete the address recognition. The XOR gate has a time window which is adjusted to the duration of the header (about 2 ps, see dashed box in Fig. 3), so only the header is processed whereas the rest of the signal is discarded. The second input to XOR gate is the local address which is synchronized with the header. The principle of the address recognition is based on the collision properties of the resonant solitons which were investigated in our previous work [1,2]. XOR gate is the key component of the header processor. The input in channel 2 of the XOR gate is set to have a phase mismatch of $\pi/2$ with the input in channel 1. In the case when the header matches the local address, the outcome of XOR gate (channel 2) is zero (see Fig. 3). If the header and the local address do not match, the outcome is nonzero and exceeds a certain threshold which is equal to half-amplitude intensity of a "1" bit pulse.

The operation of the receiver node is bit-rate flexible. To demonstrate this, the simulations have also been performed with Gbit/s optical packets. The principle of header processing in this case is the same as described above. The numerical results for a 200 Gbit/s optical bus rate are presented in Figs. 4 and 5. It should be noted that the simiulations with Gbit/s packets require to keep very large time windows for integration due to greatly increased delay time between the consequtive pulses in the packet. Therefore, a shorter packet length (6 bits) has been chosen in this case to reduce the time window and minimize the computing time.

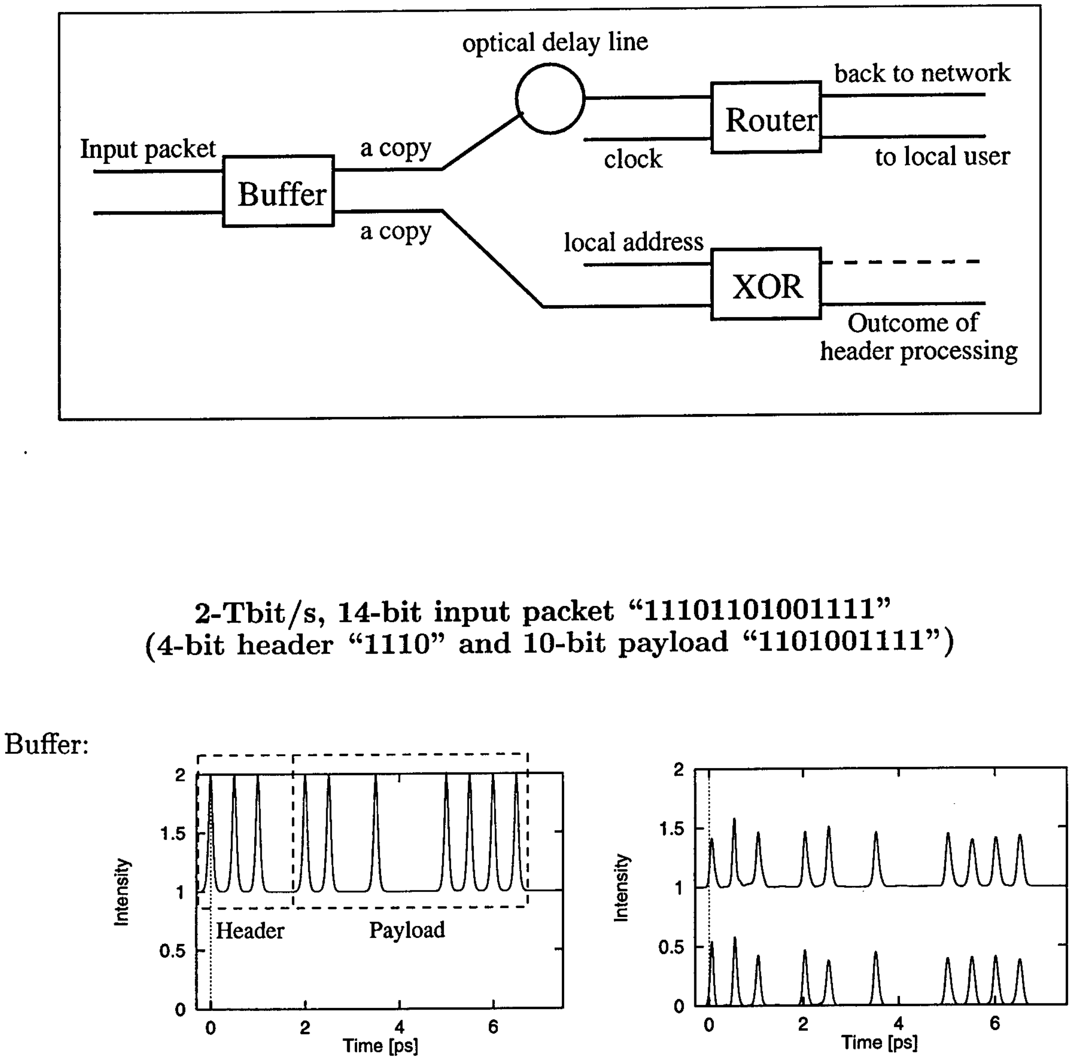

FIG. 2. Top: block diagram of the receiver node. Below: operation of a buffer in the receiver node. The input optical packet "11101101001111" (left) is transformed into two half-amplitude copies (right). One copy is directed to XOR gate for header processing, another copy is directed to the router via an optical delay line (see the next Figure).

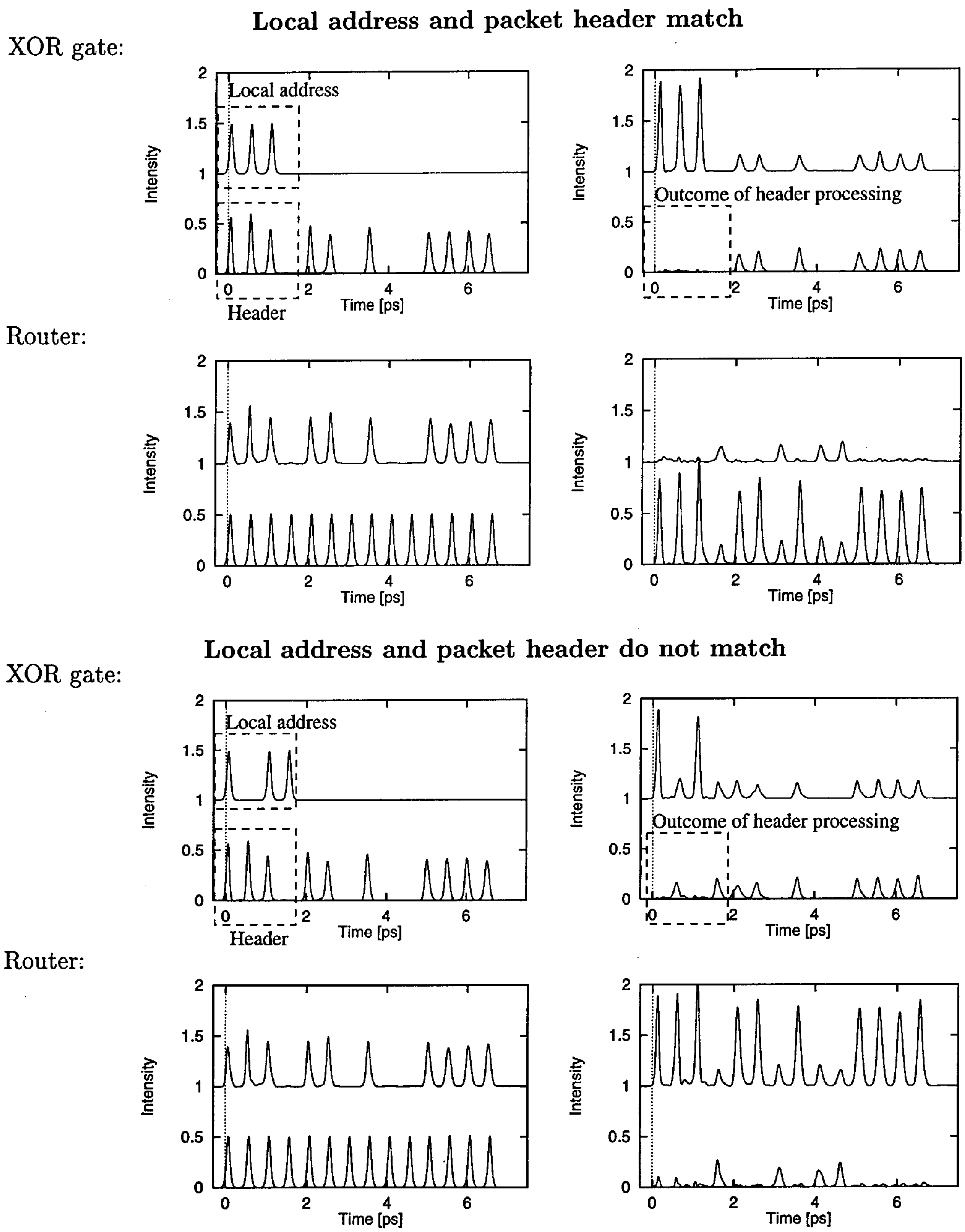

FIG. 3. Operation of the XOR gate (header processor) and the router in the receiver node. An input to the XOR gate (left) is given by a 4-bit local address and a copy of the input packet; the time window of the gate is adjusted to the header duration (dashed frame). An optical delay line is implied in the path connecting the buffer and the router where the packet is stored during the time needed to complete header processing in XOR gate. A phase of the clock pulses which enter the router is set depending on an outcome of header processing to be $+\pi/2$ or $-\pi/2$ with the input packet. When the local address and packet header match (the outcome of header processing is zero), the packet is routed to the local user (the output of the router is in channel 2); otherwise, the packet is returned back to network (the output of the router is in channel 1).

Packet routing

Depending on the result of the header processing, the second copy of the input packet which has been passing through the optical delay line untill the address recognition is completed, is then routed either to local user or back to network. The principle of packet routing is also based on the collision properties of the resonant solitons. One input to the router is a copy of the input packet, another input is a clock stream (see Figs. 3 and 5). The clock pulses are set to be $+\pi/2$ or $-\pi/2$ out of phase with the packet pulses, depending on the outcome of the header processing. As a result, the packet either remains in the same channel (back to network) or switches to another channel (to local user). A possible way to achieve the required phase shift of the clock pulses in experimental setup is to use an interferometer that is actively controlled. Setting up such an interferometer is anticipated at later stages of the related experimental investigation [7].

Note that there is generally certain degradation in the signal-to-noise ratio (SNR) for the packet content as a result of the header processing (see Figs. 3 and 5). SNR can be improved by placing an extra (cascaded) NLDC after the router to supress the low-amplitude noise in the time slots corresponding to "0" bits.

200-Gbit/s, 6-bit input packet "101011"
(3-bit header "101" and 3-bit payload "011")

Buffer:

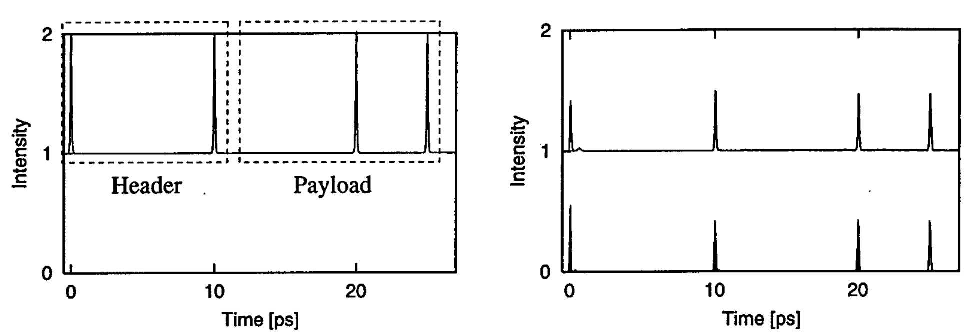

FIG. 4. Operation of a buffer in the receiver node. The input optical packet "101011" (left) is transformed into two half-amplitude copies (right). One copy is directed to XOR gate for header processing, another copy is directed to the router via an optical delay line (see the next Figure).

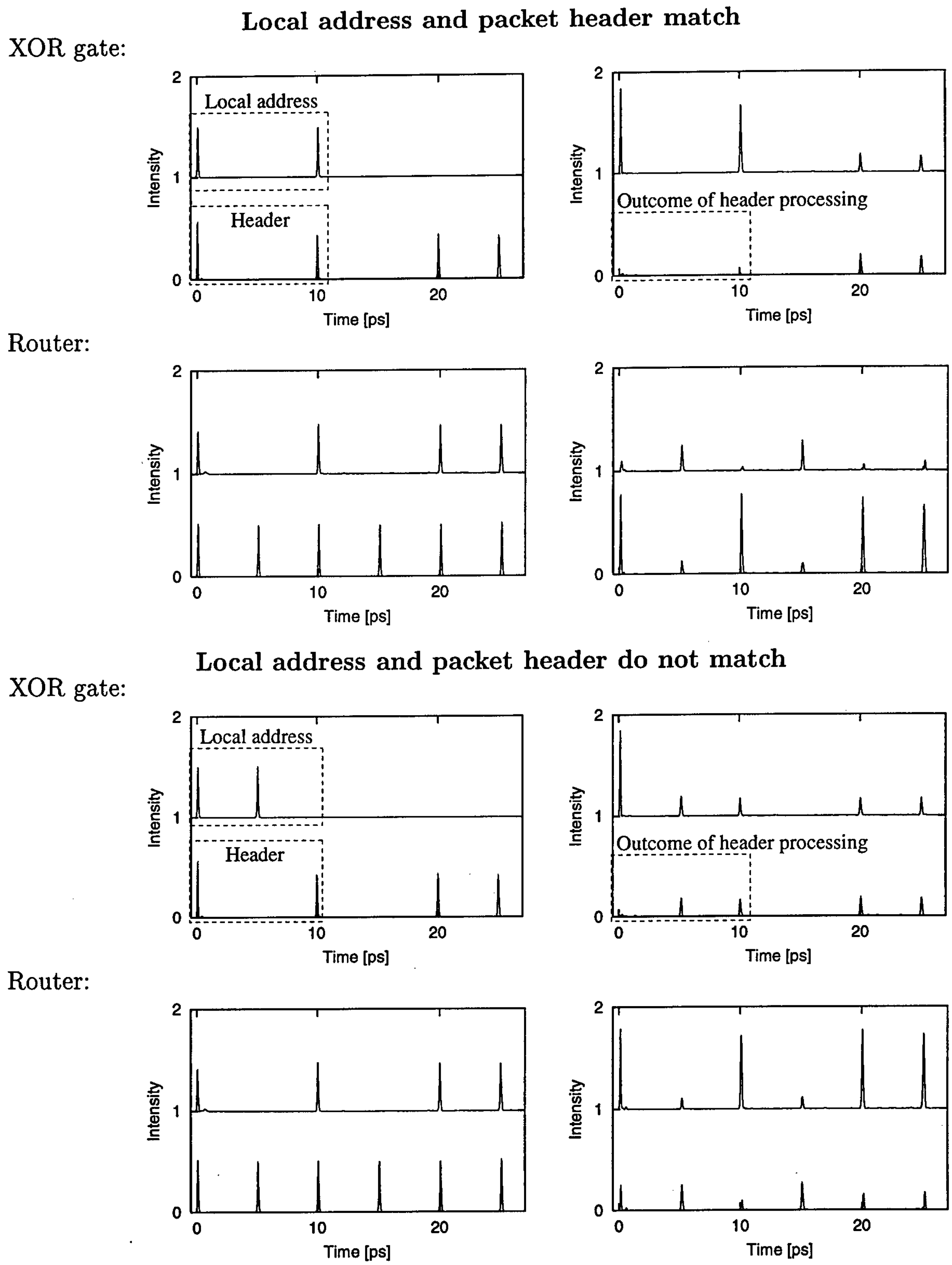

FIG. 5. Operation of the XOR gate (header processor) and the router in the receiver node.An input to the XOR gate (left) is given by a 3-bit local address and a copy of the input packet; the time window of the gate is adjusted to the header duration (dashed frame). An optical delay line is implied in the path connecting the buffer and the router where the packet is stored during the time needed to complete the header processing in XOR gate. A phase of the clock pulses which enter the router is set depending on an outcome of the header processing to be $+\pi/2$ or $-\pi/2$ with the input packet. When the local address and the packet header match (the outcome of header processing is zero), the packet is routed to the local user (the output of the router is in channel 2); otherwise, the packet is returned back to network (the output of the router is in channel 1).

Considerable simplification in the design of optical delay line can be achieved in the case of a fixed-length header. In this case, the header of each optical packet is assumed to have the same format (the same number of bits on a fixed time slot). Then, the time needed to process the header is the same for each packet, so the length of the optical delay line can be fixed accordingly. Due to low latency of XOR gate (on picosecond time scale, see Sec. 5), the required delay time should be minimal. Note that the fixed-length header scenario is most likely to be adopted in packet networks (similar to the case of fixed-length postal codes).

Buffering

Buffering of ultrafast optical data packets is an important function for future TDM networks. Optical buffers must present multiple copies of the incoming data packets to a demultiplexer or rate converter in the case when the incoming packet has been routed to a local user. In addition, the buffers should be able to hold the data packets while they wait for access to the network. This latter function requires a very complex design and can be performed with regenerative buffers employing optical logic gates [12] or the compensating fiber loop buffers [13] which have been recently proposed for TDM applications.

The operation of 2×2 buffer and the design of the optical delay line as a part of the receiver node have been discussed above. Here, we add that, to produce multiple copies of the input packet, more complex buffer configurations can be used. For example, 3×3 NLDC with approoapriately chosen length of the coupling region produces three identical copies of the input packet (see Fig. 6). Note that each copy has 1/3 of the intensity of the input packet. The simulations have been performed with a 3-Tbit/s input packet (Fig. 6a) and a 500-Gbit/s input packet (Fig. 6b) to demonstrate that the buffer operation is bit-rate flexible and the performance is the same in the case of different rates. A similar approach can be used to implement an optical buffer which produces N copies of the input packet. This buffer would be practical to operate in conjunction with a rate converter in the case when the input packet has been routed to a local network of N lower rate users.

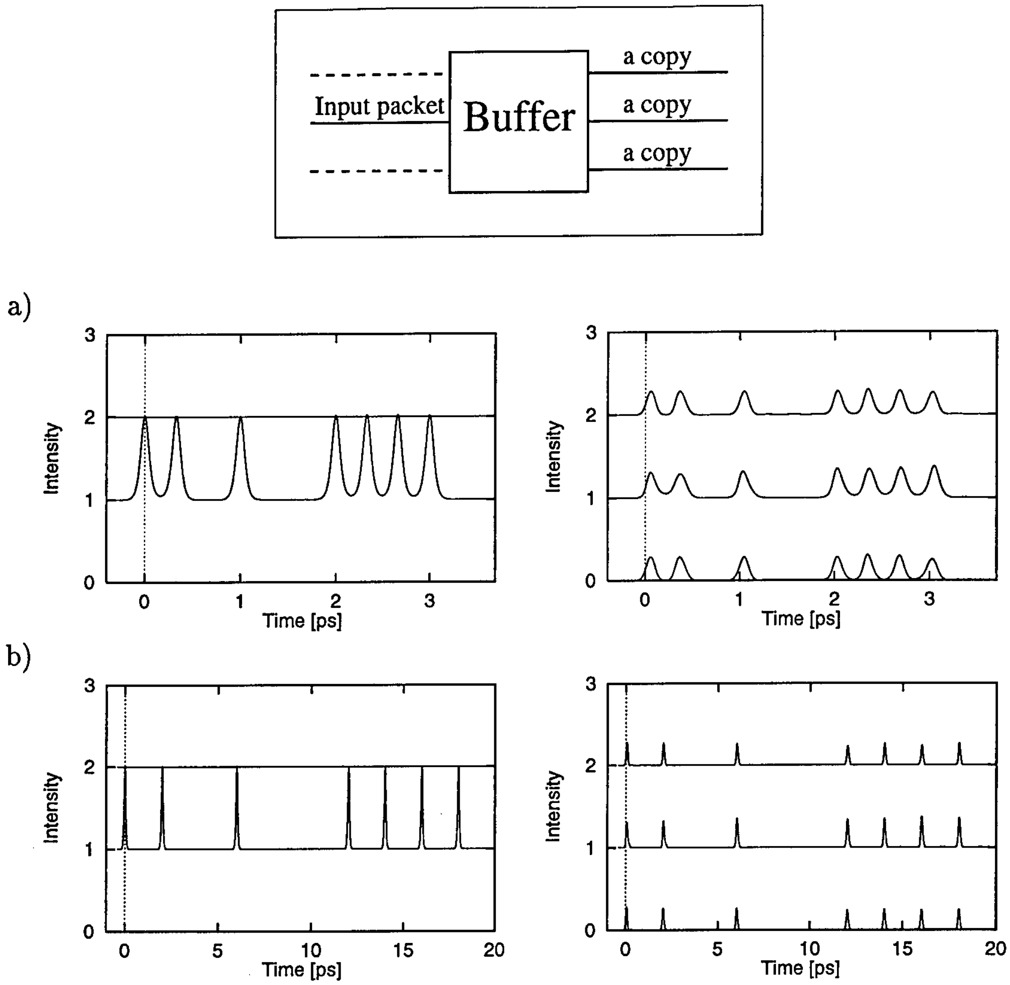

FIG. 6. Top: schematic of a 3×3 buffer. Below: operation of the buffer. (a) The input optical packet "1101001111" with a bit rate 3 Tbit/s (left) is transformed into three smaller-amplitude copies (right); (b) the same as in (a) except the bit rate is 500 Gbit/s.

Clock recovery

A method which allow all-optical signal amplification in the resonant soliton scheme has been described in our recent work [2]. It is based on the collision properties of the resonant solitons. The gain factor can be adjusted by varying the amplitude of the control (clock) pulses (see Fig. 1 in Ref. [2]). Implementation of the same method for clock recovery in the receiver node requires additional hadrware including a cascaded NLDC, a source of optical clock, and the techniques for pulse synchronization and optical phase control. Note that these are the same techniques that are involved in operation of other components of the node, such as the header processor and the router.

Data rate conversion

In networks servicing a heterogeous user population, all users may not generate or accept data at the ultrafast bus rate. Therefore, a rate conversion between the ultrafast optical bus and lower rate local streams may be required at the user access nodes. For example, if the incoming packet address matches the local address for a lower rate user, the data packet must be stored and its rate must be converted down to the local user rate. Realization of data rate conversion for the input packets of arbitrary formats is a challenging task.

First, we consider a case of optical clock streams in which the rate conversion can be performed in a relatively simple way. Namely, we demonstrate a scheme which allows to up-convert the bit rate of the clock streams (optical clock repetition-rate multiplication). This case is of practical interest because high-repetition-frequency optical clock sources are one of the key components required for ultra-high-speed optical communication networks. Due to technical complexity of increasing the repetition rate of the laser source itself, it is more sensible to use an external rate multiplier.

Let us consider a 250-Gbit/s optical clock stream which is split into two streams (see Fig. 7). These two streams serve as inputs to the rate converter 1. This rate converter is a resonant soliton NLDC with the length of the coupling region $d = L_c/2$ (L_c is the coupling length). The only requirement to achieve the rate multiplication is that the input 2 (clock 2) has to be time delayed by $t_d = \Delta t/2$ via an optical delay line (Δt is the time delay between two subsequent pulses in the stream). In the rate converter 1, each clock stream half-couples between two channels, so the outcome is two half-amplitude streams with a bit rate 500 Gbit/s. Thus, each rate converter doubles the repetition rate of the input clock stream. Further rate multiplication can be achieved by cascading the rate converters. For example, the output of the rate converter 1 can serve as an input to the rate converter 2 provided that the clock 2 has been time delayed approapriately ($t_d = \Delta t/4$). This second rate converter is identical to the first one, and it produces two 1-Tbit/s half-amplitude clock streams. This procedure can be repeated again if further rate up-conversion is required. Note that a $2N$ increase in the repetition-rate of the clock stream is accompanied by a $2N$ reduction in the amplitude of each pulse in the stream where N is the number of cascaded rate converters.

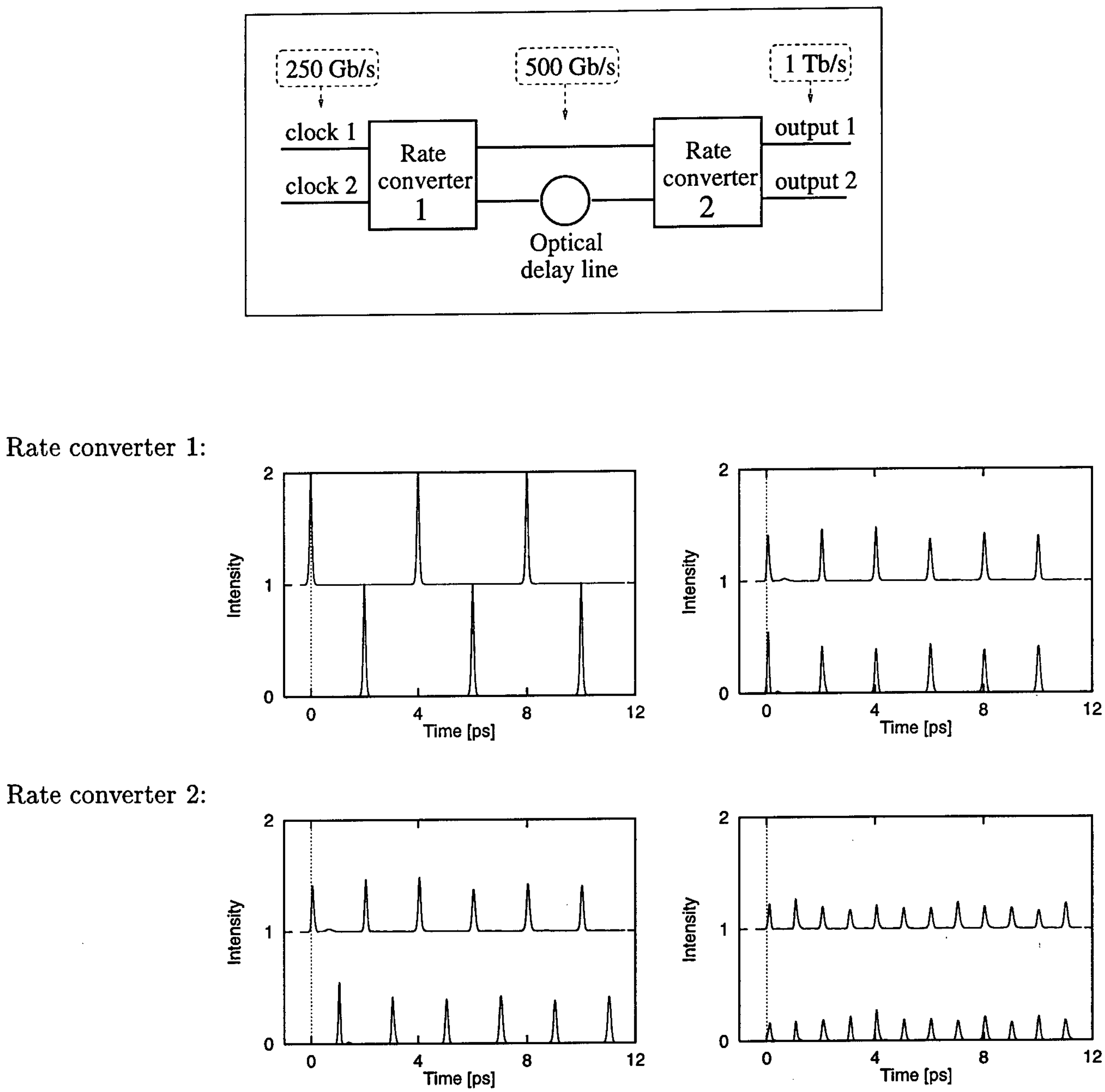

FIG. 7. Top: schematic of a cascade of two rate converters. Below: operation of the rate converters. The inputs to the converter 1 (left) are identical clock streams with a bit rate 250 Gbit/s, a time delay between the inputs is $\Delta t = 2$ ps; the outputs (right) are two half-amplitude clock streams with a bit rate 500 Gbit/s. These outputs serve as the inputs to the rate converter 2 after the stream in channel 2 passes through an optical delay line resulting in $\Delta t = 1$ ps; the outputs are two half-amplitude clock streams with a bit rate 1 Tbit/s.

The proposed optical clock repetition-rate multiplication scheme is phase and polarization insensitive and can be implemented in conjunction with available sources of optical pulse trains, such as mode-locked semiconductor lasers, etc. Compared with other multiplication techniques [14,15], the scheme proposed here is conceptually simple and compact.

Another issue of interest is a possibility to achieve the rate down-conversion in the case of optical packets of an arbitrary format. In contrast to the example above, the resonant soliton scheme does not offer any conceptually simple solution in this particular case. In fact, a possible scheme for the rate down-conversion involves a wavelength coding which cannot be modelled with the existing numerical code. The scheme exploits the so-called recirculating photonic filter that can realize true-time delay for wavelength coded bit streams [16]. The basic requirement for operation of this device is that each bit in the input stream must be first coded with a different optical carrier wavelength, λ. Then, an arrayed-waveguide grating steers each optical carrier to the approapriate integrated delay line, depending on the carrier wavelength (see Fig. 8). The symmetric feedback (recirculating) configuration consists of optical fibers of different lengths connected among symmetric pairs of input and output ports of the device. This configuration allows to implement the desired time delay for each signal which is then fed back into the symmetric input port. The grating then focuses the delayed bits into the common output port.

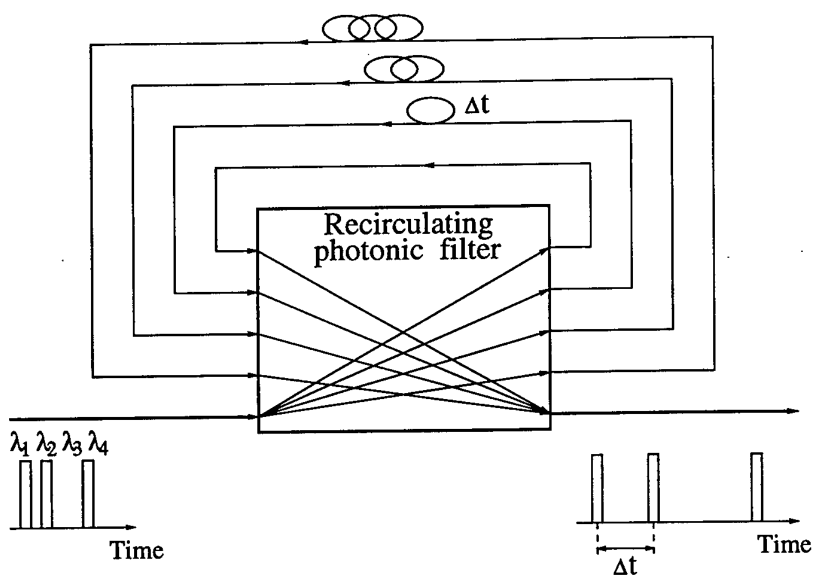

FIG. 8. Schematic of a recirculating photonic filter operation. A wavelength coded input "1101" has been stretched in time.

To implement the above technique for rate down-conversion in the TDM receiver node, it is first necessary to encode each bit in the optical packet payload with a different carrier wavelength. The methods which allow the required λ coding, are available (see, for example, Ref. [17]). While the overall process of data rate down-conversion features significant technical complexity, it does allow to achieve the required reduction in the data rate.

Demultiplexing

Demultiplexing of clock stream can be required for performing certain tasks in the packet networks. Here, a particular example of demultiplexing is presented, namely, when every fourth pulse is eliminated from a 3 Tbit/s clock stream by the control pulses in channel 2 (see Fig. 9a). As a result, the output (channel 2) is given by a sequence of 3-bit packets separated by empty time slots. This function is achieved with a single 2×2 NLDC where the control pulses are $\pi/2$ out of phase with the signal pulses. Note that the amplitude of the output pulses in channel 2 is two times smaller than the amplitude of the input pulses.

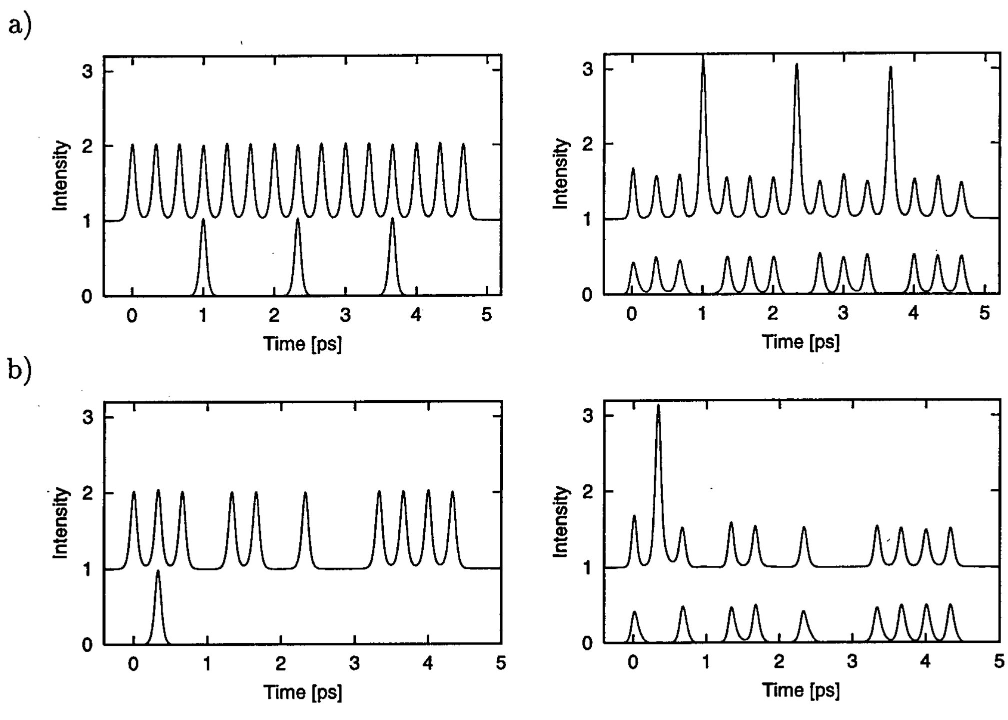

FIG. 9. Operation of a demultiplexer. (a) The input is given by a 3-Tbit/s optical clock stream in channel 1 (left). The control pulses in channel 2 (a lower rate synchronized clock) eliminate every fourth pulse in the stream. The output is "111011101110111" in channel 2 (right). (b) The input is given by a 3-Tbit/s optical packet "11101101001111" in channel 1 (left). The control pulse in channel 2 removes the second bit in the packet. The output is "101011101110111" in channel 2 (right).

A single control pulse can be used to eliminate a particular bit in the optical packet using the same scheme as in Fig. 9a. An example is presented in Fig. 9b where the second bit in the incoming packet "11101101001111" is removed by the control pulse. Note that a similar technique can be used to add a "1" bit to an empty time slot in the packet.

5. Operating characteristics of the components in the receiver node

Switching speed

The main objective of the performed simulations has been to demonstrate a possibility of optical packet processing in Tbit/s regime. As seen in Figs. 2 and 3, the receiver node is capable to operate at data rates of 2 Tbit/s. This is certainly not the upper limit for the node throughput. The maximum operating speed, however, is limited by two major factors. On the one hand, the time delay between the consequtive input pulses must be longer than 3τ where τ is the pulse duration, otherwise, the device performance degrades considerably due to pulse overlaping. In the case $\tau = 100$ fs which has been chosen in our numerical simulations, the maximum operating speed of the gates is ~ 3 Tbit/s. The operation of a buffer (Fig. 3) and a demultiplexer (Fig. 9) at the clock rates of 3 Tbit/s have been demonstrated.

A higher processing speed of the node can be achieved with a shorter input pulse duration. For example, if $\tau = 30$ fs, the node throughput can be as high as 10 Tbit/s. There is, on the other hand, a limit on τ values which is implied by the choice of a particular semiconductor material used to fabricate the constituent waveguides of NLDC: the spectral width of the input pulses must be smaller than the binding energy of the excitonic transition of interest, otherwise, an excitation of the continuum states leads to rapidly increasing dephasing rates which degrade the operating performance of switches and logic gates. In the case of II-VI CdZnTe/ZnTe MQWs, the exciton binding energy is ≈ 23 meV [9] which is large enough to allow the use of 100 fs input pulses. In the case III-V GaAs/AlGaAs MQWs, the typical values of the exciton binding energy is smaller than 10 meV [9,10].

The bit-rate flexibility of the resonant soliton scheme is a great advantage for potential applications. For example, highly efficient operation of the switches and logic gates in Gbit/s regime

means that these devices can be of immediate use in the currently existing optical networks where the data transmission rates are still well below Tbit/s range. As seen from Figs. 4 and 5, the operation of the receiver node in the case of 200 Gbit/s optical packets is similar to that in Tbit/s regime.

Switching contrast

As shown in our previous work, the resonant soliton scheme inhibits incomplete pulse switching [1]. This feature ultimately leads to high switching contrast ratio. Indeed, in the simulations, the SNR value is about 10 for the resonant soliton switches and is generally in the range 4–10 for the logic gates. These are values without account for the polarization dephasing rate, γ_2, which leads to a decrease in SNR.

Switching energy

The crossover pulse area for switching in the case of 100 fs input pulses and II-VI CdZnTe/ZnTe MQWs material parameters parameters is 0.6π (see Fig. 3 in Ref. [1]). The pulse area of the standard "1" bits has been chosen to be 2π in our simulations. The corresponding pulse energy can be calculated if the value of the transition dipole moment is known. From relevant experimental results on soliton-like propagation of femtosecond optical pulses in the excitonic spectral region of bulk CdSe [18], some numbers can be obtained. A set of measurements in Ref. [18] has been performed with 180 fs pulses, and the typical input pulse intensities have been 46 $\mathrm{MW/cm^2}$ ($\sim 2\pi$ pulse area) and 26 $\mathrm{MW/cm^2}$ ($\sim 1.5\pi$ pulse area). Note that these results have been obtained in 3D case and therefore cannot be quantitatively applied to 2D case which is of interest here. The other relevant experimental results have been reported in Ref. [10] where subpicosecond optical switching in GaAs/AlGaAs NLDCs with current injection has been studied. The results of a few measurements without injected current in the resonant excitation regime indicate that, in the case of GaAs/AlGaAs MQWs, the required pulse energy for the resonant switching should be within the range 10–20 pJ.

Latency time

The latency time of a single resonant soliton switch depends not only on the device length, but also on the input pulse duration, τ. The latter dependence occurs because the group velocity

of the propagating pulse under the resonant excitation conditions depends on τ: a shorter pulse propagates faster (see, for example, Ref. [19]). Assuming that the length of the coupler is 2 mm and the input pulse duration is 100 fs, the latency time of the device is about 100 ps. Thus, the resonant soliton switches have extremely low latencies.

Device size

An important feature of the resonant soliton switches and logic gates is their compactness. The typical device length for a semiconductor NLDC is about 1–2 mm, a width of the constituent waveguides is about 3 μm, and the spacing between them is 2 μm (see, for example, Ref. [10]). These semiconductor devices are attractive from an applications viewpoint because they are so compact and may be completely integrated using photonic integrated circuit technologies.

Limitations on device operation

There are two main limitations on operation of the resonant soliton switches and logic gates. The first one is that the operating wavelength of these devices is determined by the wavelength of the corresponding excitonic transition and therefore depends on the choice of the semiconductor material to implement the device. To fabricate the devices which permit operation in the spectral region around the optical communication wavelength (1.55 μm), semiconductor materials which have excitonic transitions in this region must be used. Note that such materials are available.

Another limitation is that the resonant soliton scheme specifically applies to ultrashort (femtosecond) optical pulses (which are always the case in Tbit/s regime) and is not suitable for switching of long optical pulses. When applications in Gbit/s optical processing are anticipated, the duration of individual pulses must still be ultrashort.

Appendix: The latest advances in Tbit/s optical switching

Significant advance in all-optical switching was achieved earlier this year by the researchers at Optoelectronics & High Frequency Device Research Laboratories, NEC Corporation, Japan, using polarization-discriminating symmetric Mach-Zehnder (PD-SMZ) all-optical switch [6]. The switching time of 200 fs and demultiplexing of 1.5 Tbit/s were reported, showing the applicability of the SMZ switches to optical demultiplexing of over 1 Tbit/s for the first time. The operation of the SMZ switches is based on a highly efficient, but slowly relaxing band-filling effect under resonant excitation conditions in a passive InGaAsP bulk waveguide. In the SMZ scheme, a signal pulse which has the wavelength in the transparency region of the semiconductor waveguide, experiences a nonlinear phase shift due to carrier density change caused by the absorption of a control pulse. Using carefully timed control pulses, the switching and demultiplexing can be achieved on the time scale which is much shorter than the relaxation time of the excited carriers. Indeed, the demonstrations were performed with a sequence of three signal 130-fs pulses [6]. On a longer time scale, the operation of SMZ switch is expected to degrade considerably due to effects of carrier relaxation. Therefore, the true high-repetition capability (operation with the pulse trains consisting a large number of signal pulses) appears to be extremely difficult to achieve with the SMZ scheme in its present form. Nevertheless, the NEC results represent a very important step towards future Tbit/s optical technologies.

Another experimental program on Tbit/s optical switching was initiated in Tucson, Arizona, in September, 1999 [7]. This program aims on fabrication and testing of the resonant soliton switches. This is the first experimental investigation of the resonant soliton scheme for switching in a semiconductor NLDC. Note that the evidences of the resonant soliton formation in bulk semiconductors have been recently reported [18,20] (in good agreement with the theoretical predictions [8]). The resonant soliton scheme is conceptually different from the SMZ approach and has no limitations on high-repetition operation of the switch [1,2]. This is exactly the feature which opens up a possibility of using the resonant soliton switches and logic gates for applications in Tbit/s optical packet processing.

Summary

- Various approaches to optical packet processing have been discussed.
- A feasibility to construct a receiver node using the resonant soliton switchies and logic gates has been demonstrated; the model receiver node includes a buffer, an optical delay line, a XOR gate, and a router.
- The address recognition function for incoming optical packets has been performed at 2 Tbit/s and 200 Gbit/s data rates to demonstrate bit-rate flexibility of the node operation. Two different cases have been considered: (i) the incoming packet address and the local address match, (ii) the incoming packet address and the local address do not match.
- Buffering of optical packets to produce multiple copies of the input has been performed using 3×3 NLDC configuration; the simulations have been performed at two different data rates: 500 Gbit/s and 3 Tbit/s.
- The clock recovery function has been discussed.
- A simple scheme to upconvert a bit rate of clock streams has been proposed, and the rate up-conversion from 250 Gbit/s to 1 Tbit/s has been demonstrated numerically.
- A possible scheme to achieve the rate down-conversion in the case of optical packets of arbitrary format has been described.
- The examples of demultiplexing of optical clock streams and optical packets at 3 Tbit/s have been presented.
- Quantitative assessment of operating characteristics of the components in the model receiver node has been performed.

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